

FIG. 1A

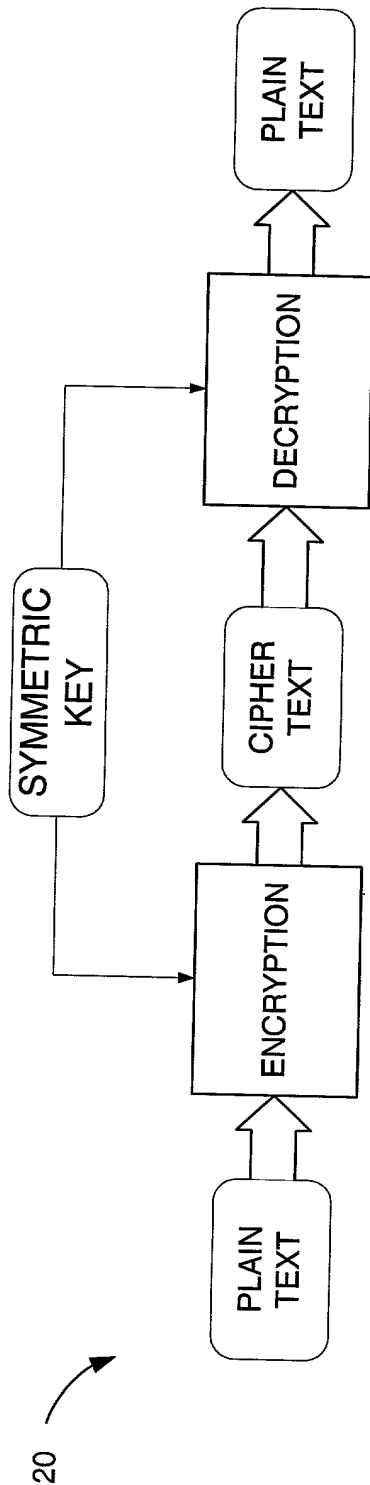


FIG. 1B

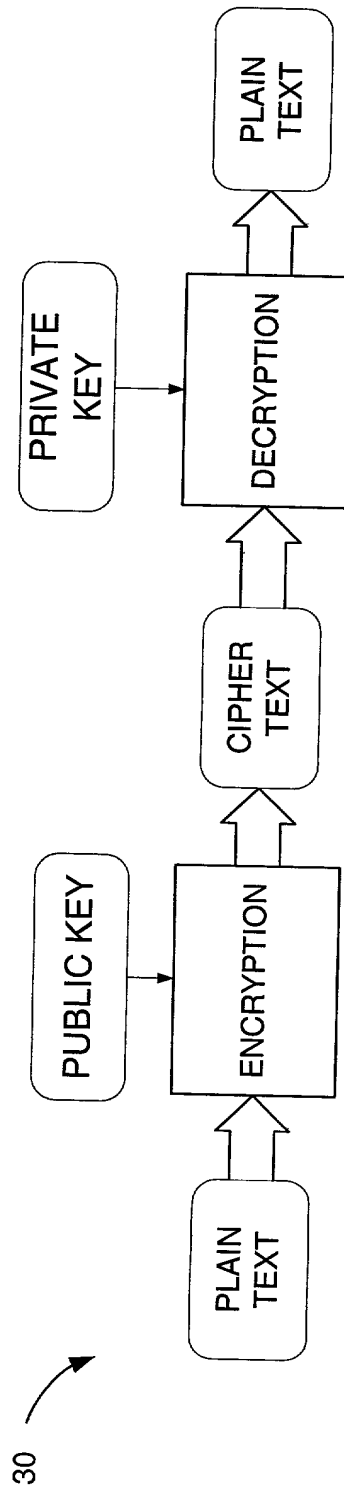
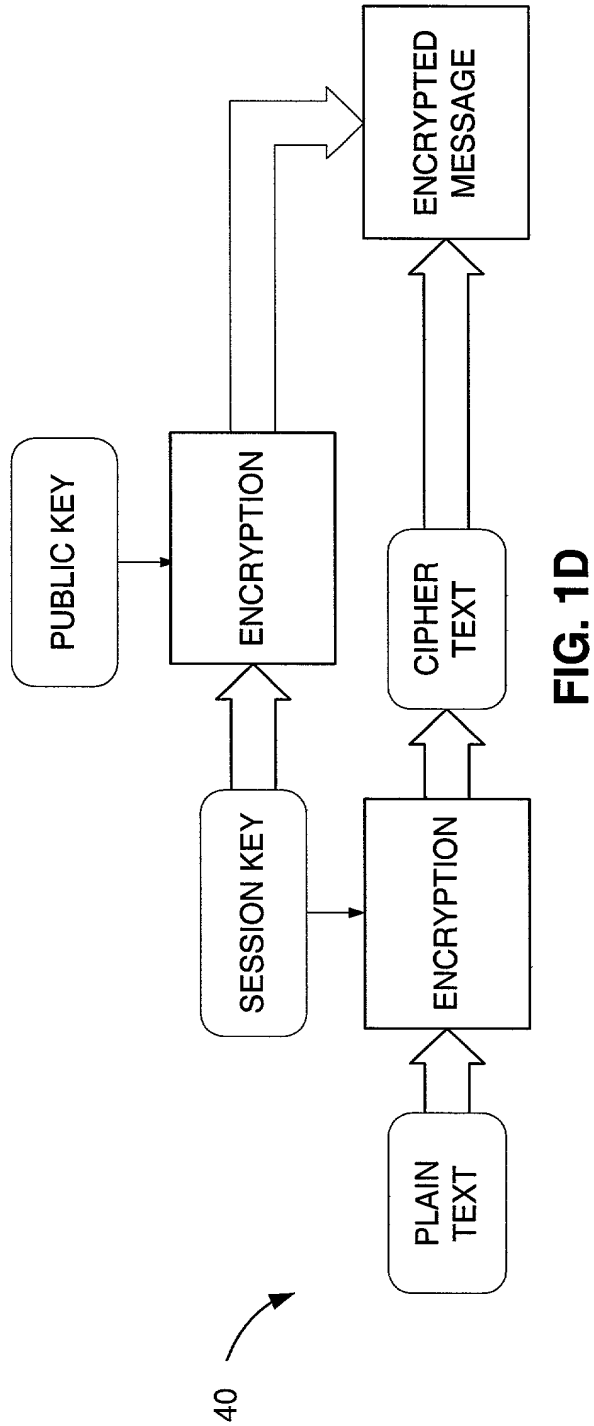


FIG. 1C

Sheet 2/ 15



Sheet 3/ 15

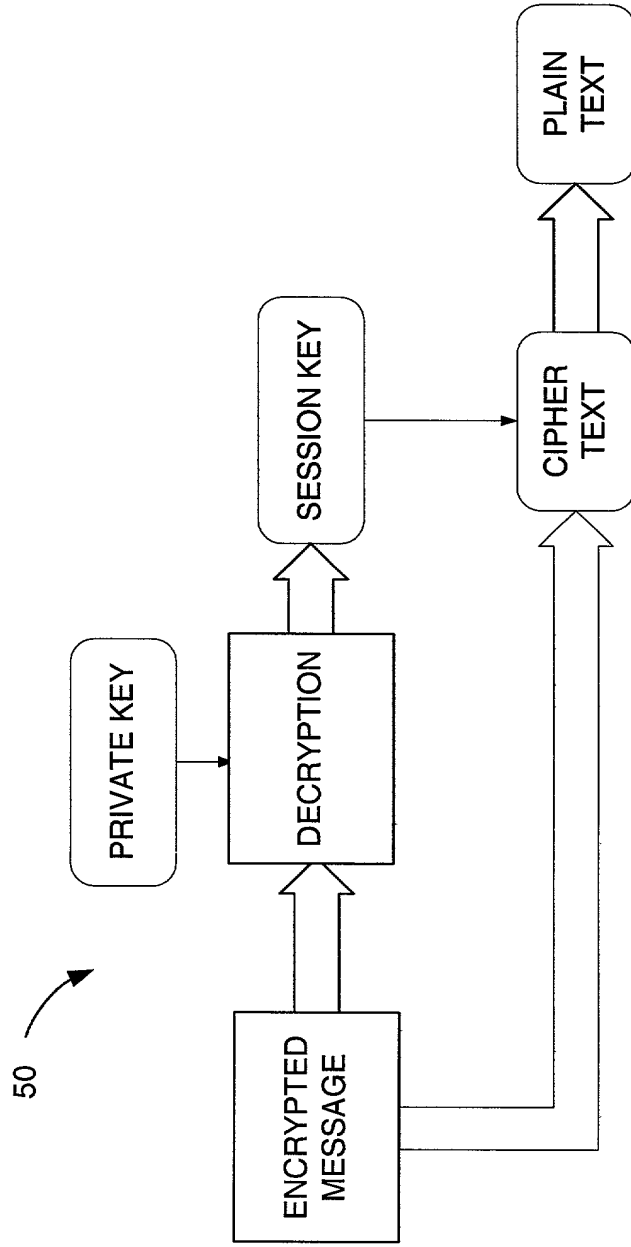


FIG. 1E

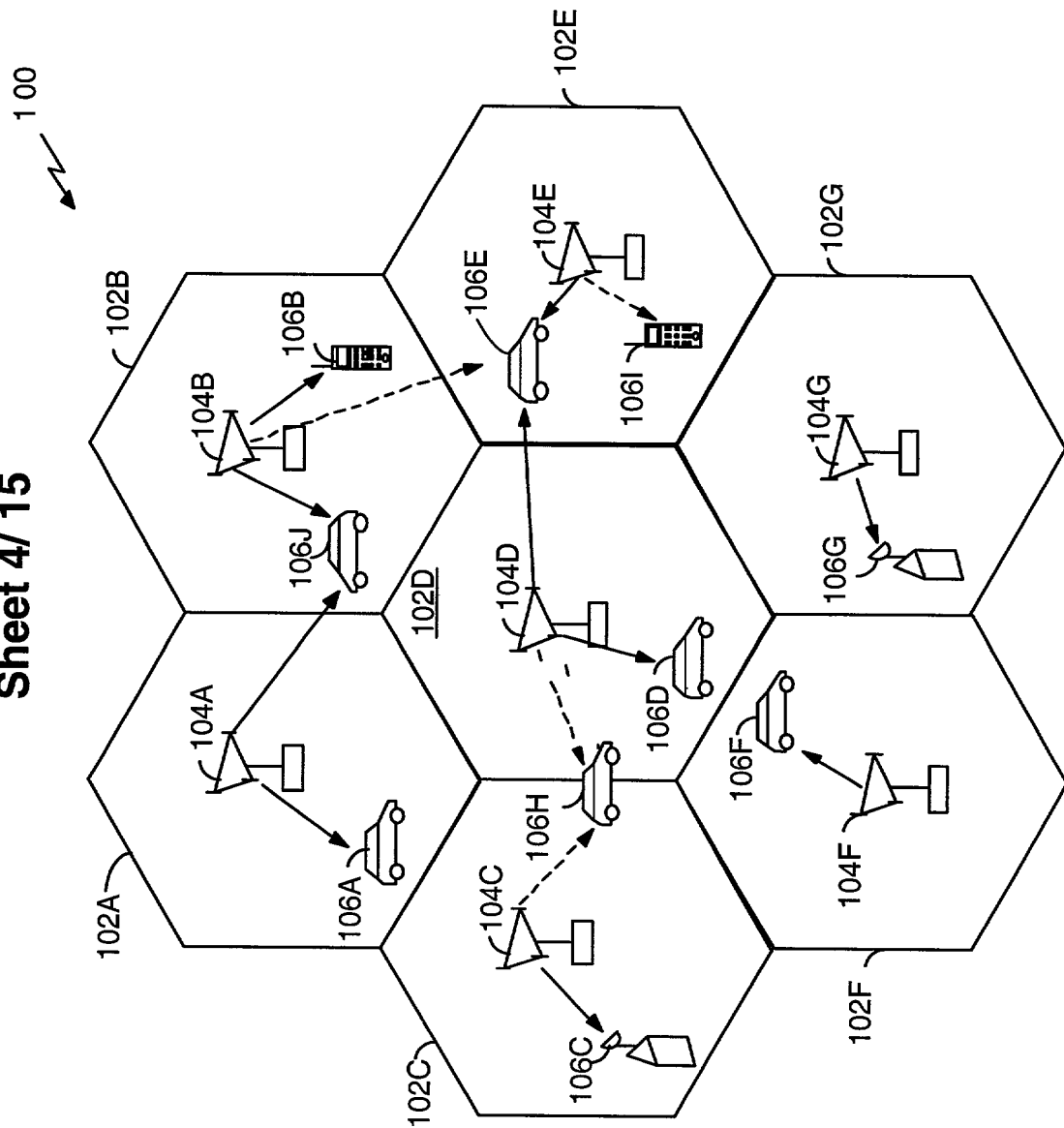


FIG. 2

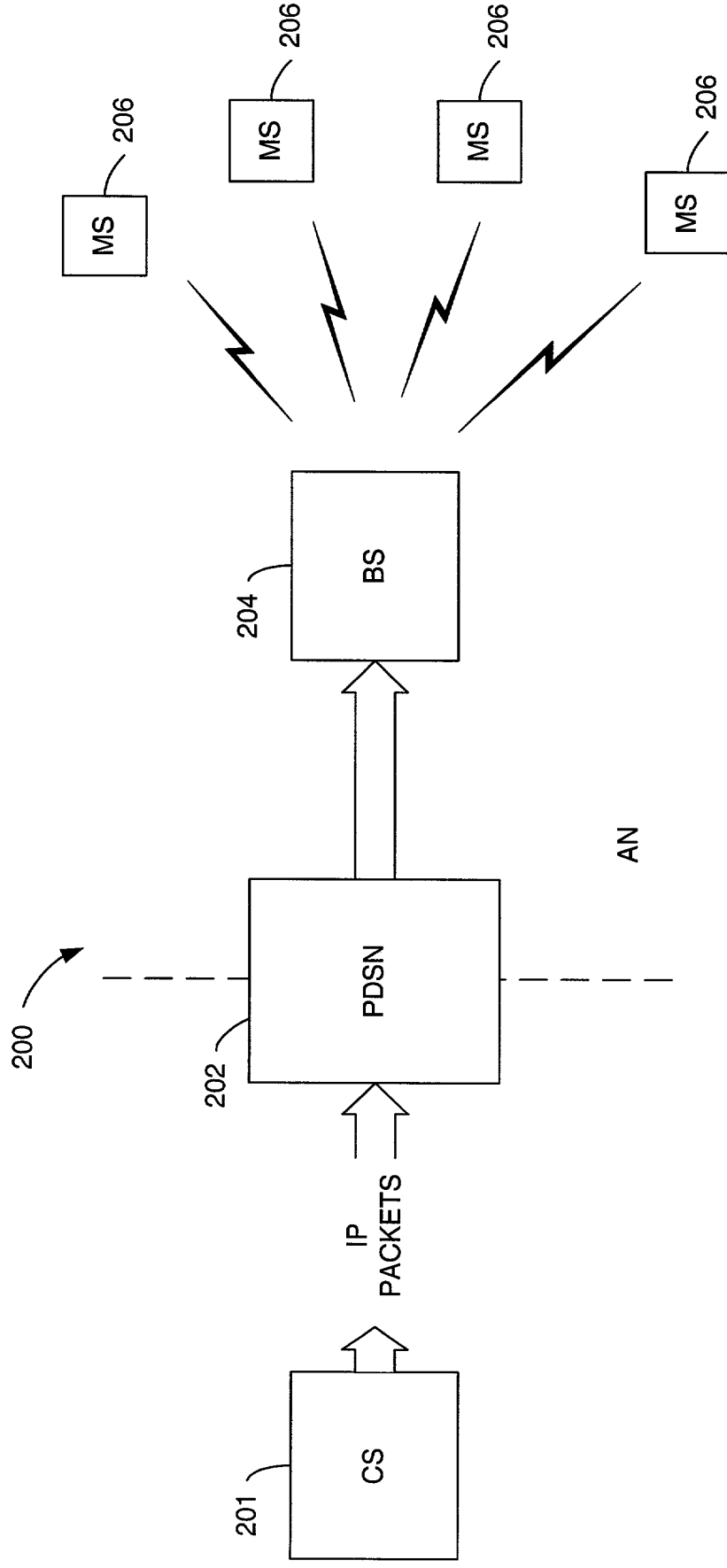


FIG. 3



FIG. 4 is a block diagram of a system 300 for processing encrypted data. The system 300 includes a receive circuitry 304, a processing unit 312, and a memory unit 306. The receive circuitry 304 is connected to an antenna 302 and receives encrypted data. The encrypted data is then processed by the processing unit 312. The memory unit 306 is connected to the processing unit 312 and stores data. The system 300 also includes a user interface module (UIM) 308, which contains a user interface processor (SUPU) 314 and a user interface memory (SUMU) 314. The UIM 308 is connected to the processing unit 312 via a system bus (SK) 316. The processing unit 312 is also connected to the memory unit 306 via a bus (BC) 310.

Sheet 6/ 15

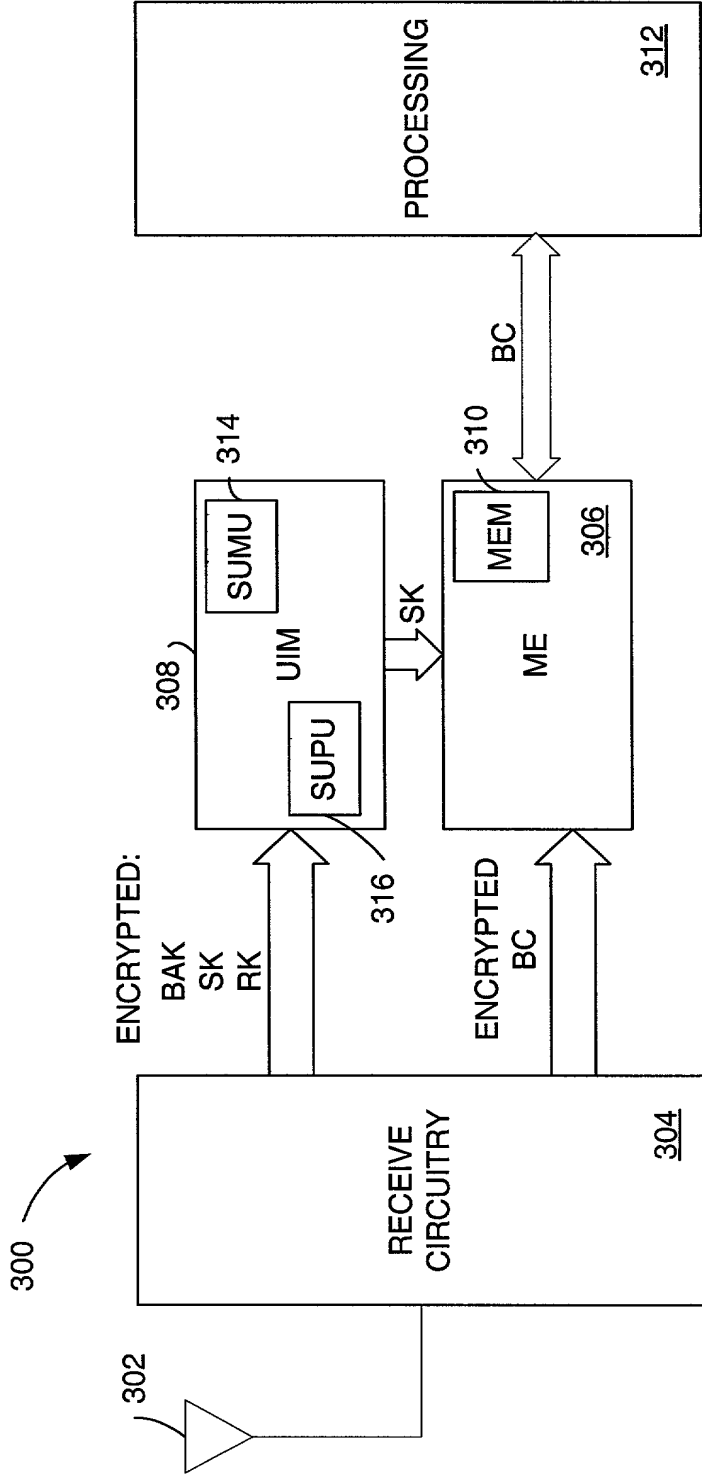


FIG. 4

Sheet 7/15

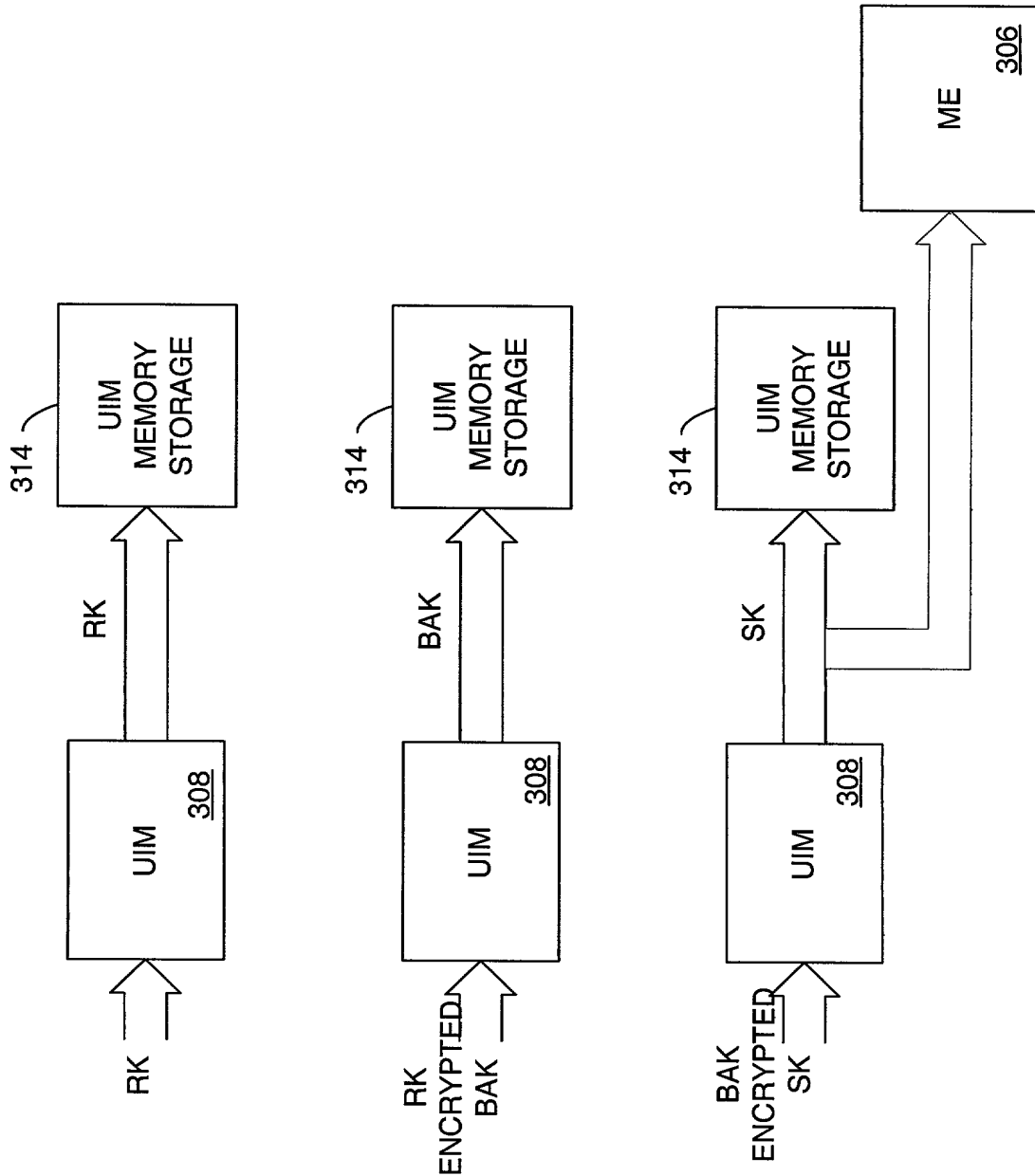


FIG. 5

500

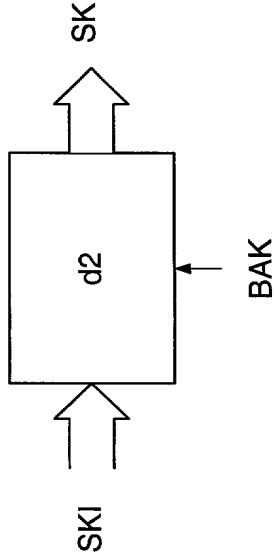
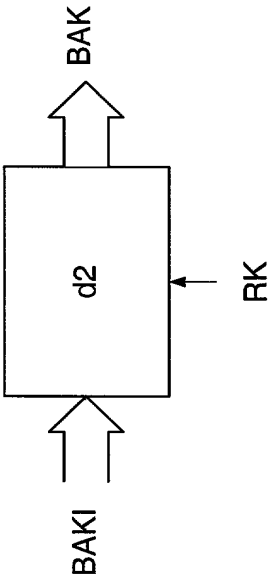
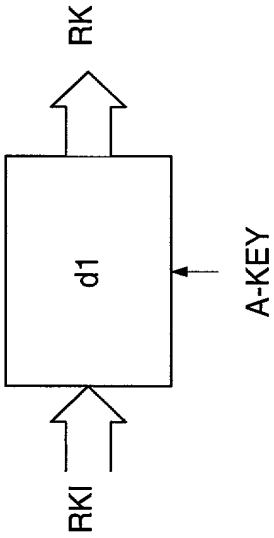


FIG. 6

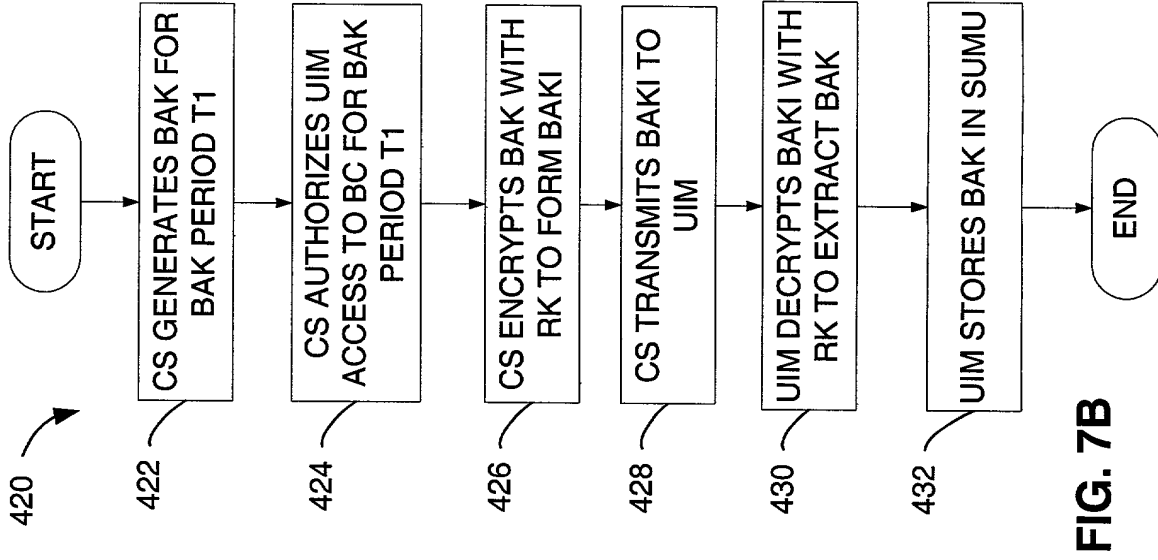


FIG. 7B

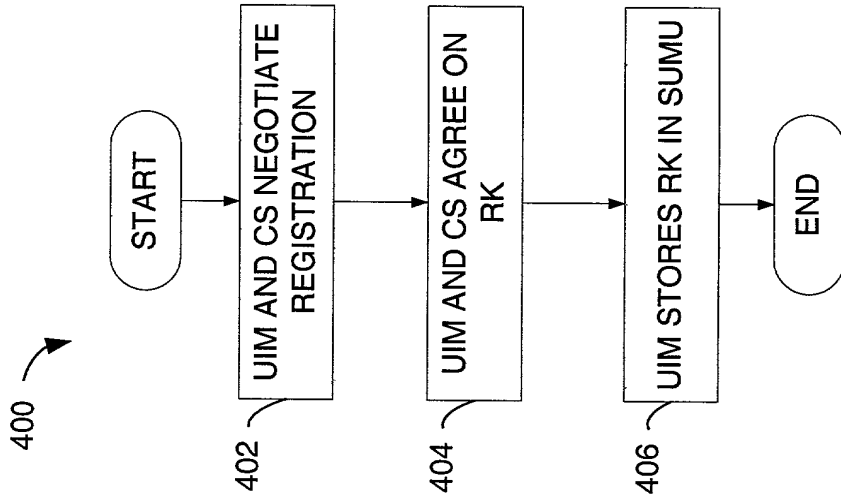
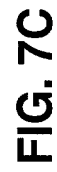


FIG. 7A



Sheet 11/15

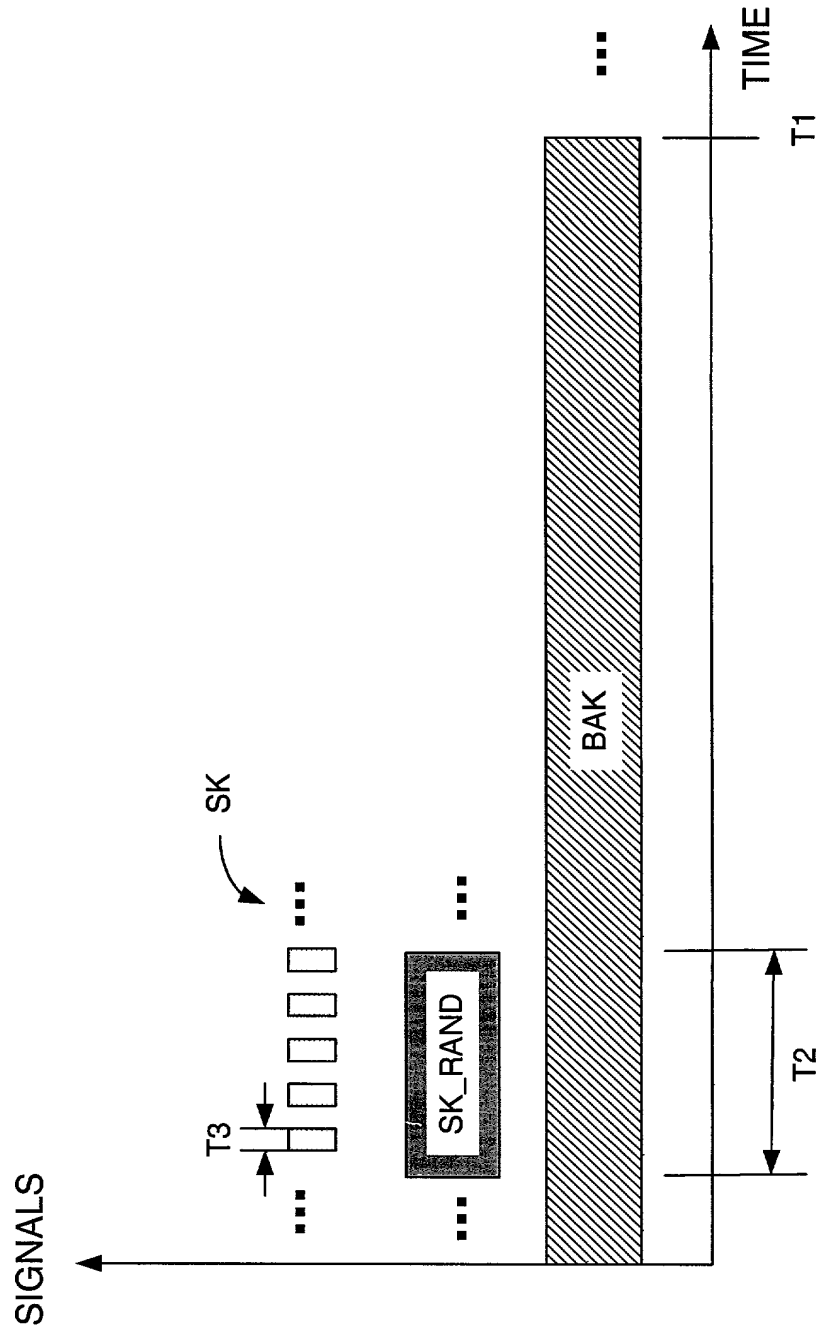


FIG. 7E

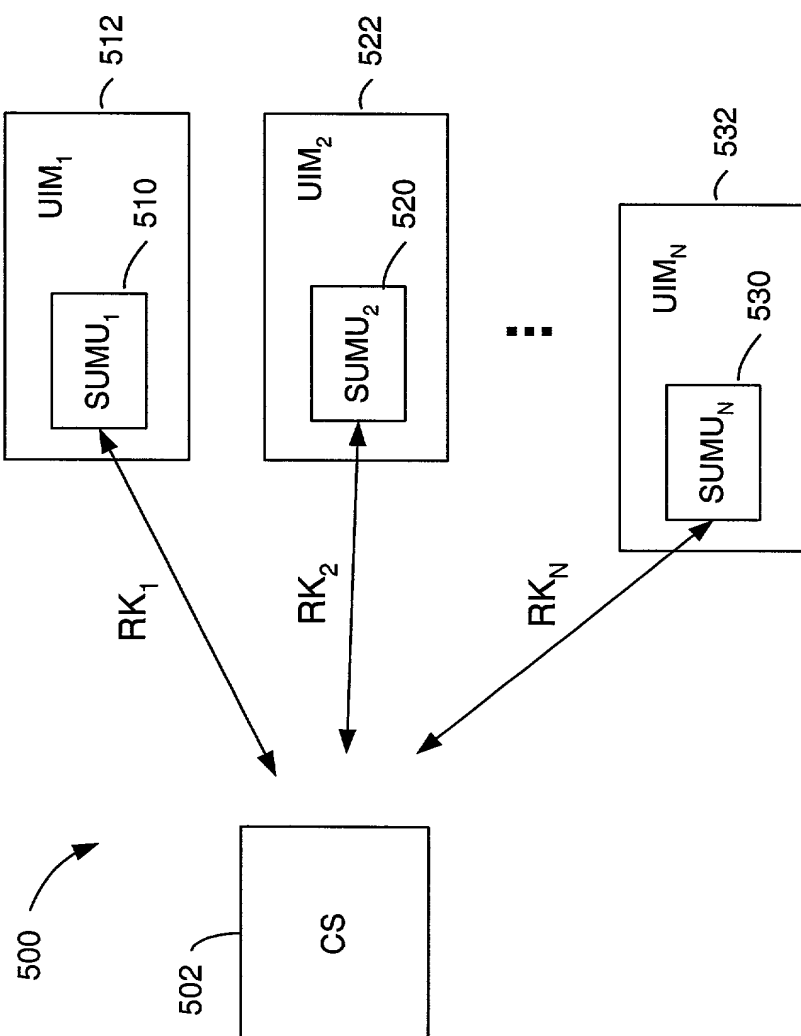


FIG. 8A

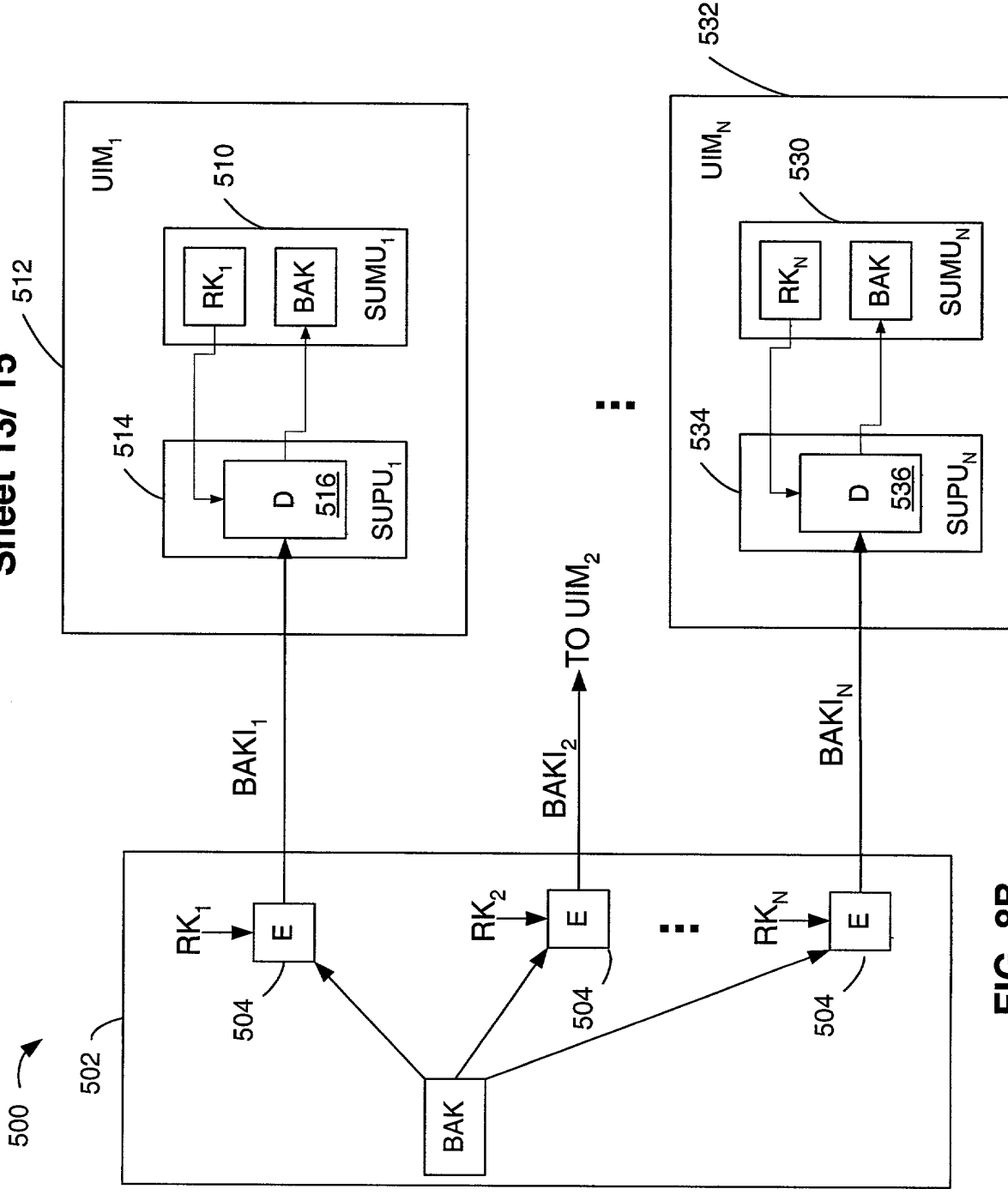


FIG. 8B

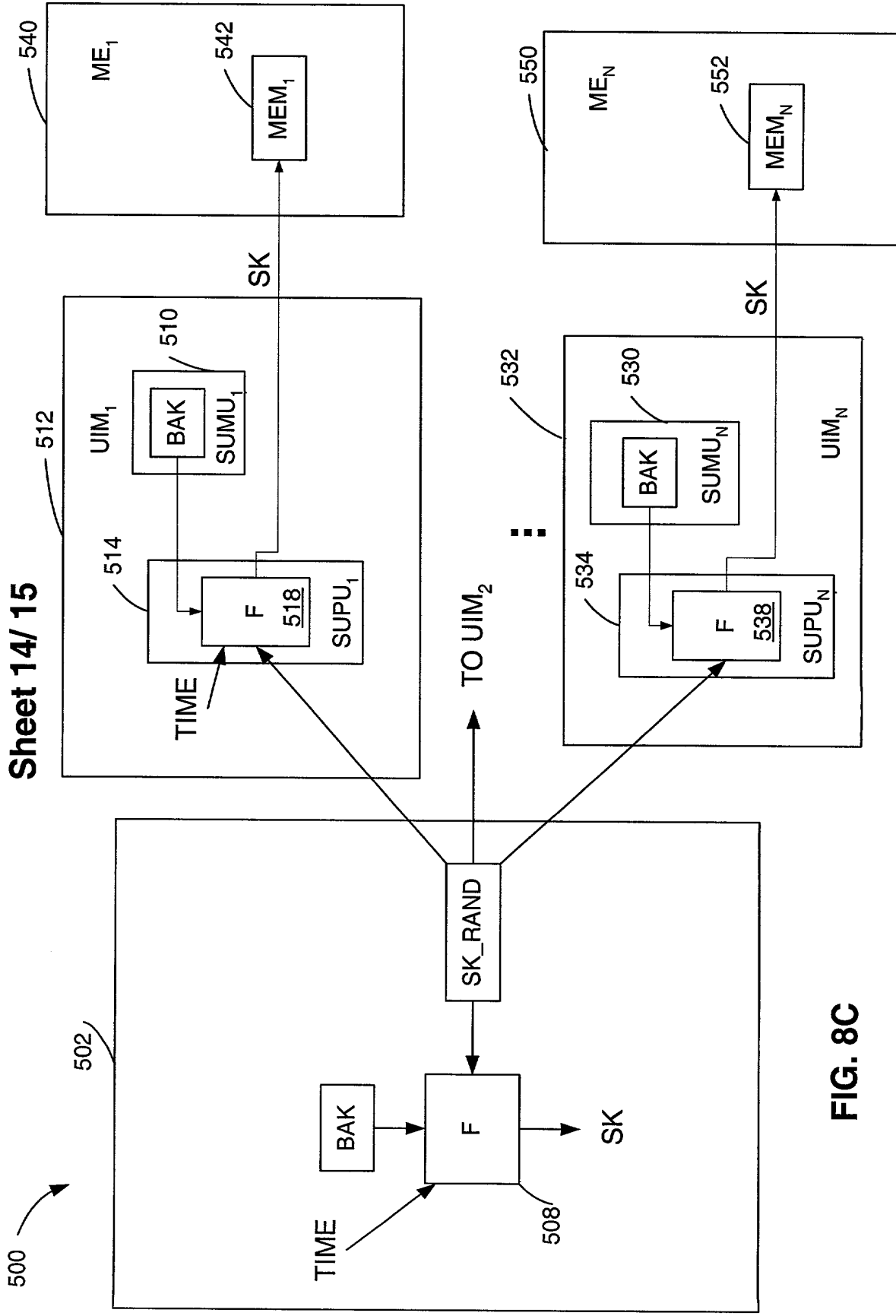


FIG. 8C

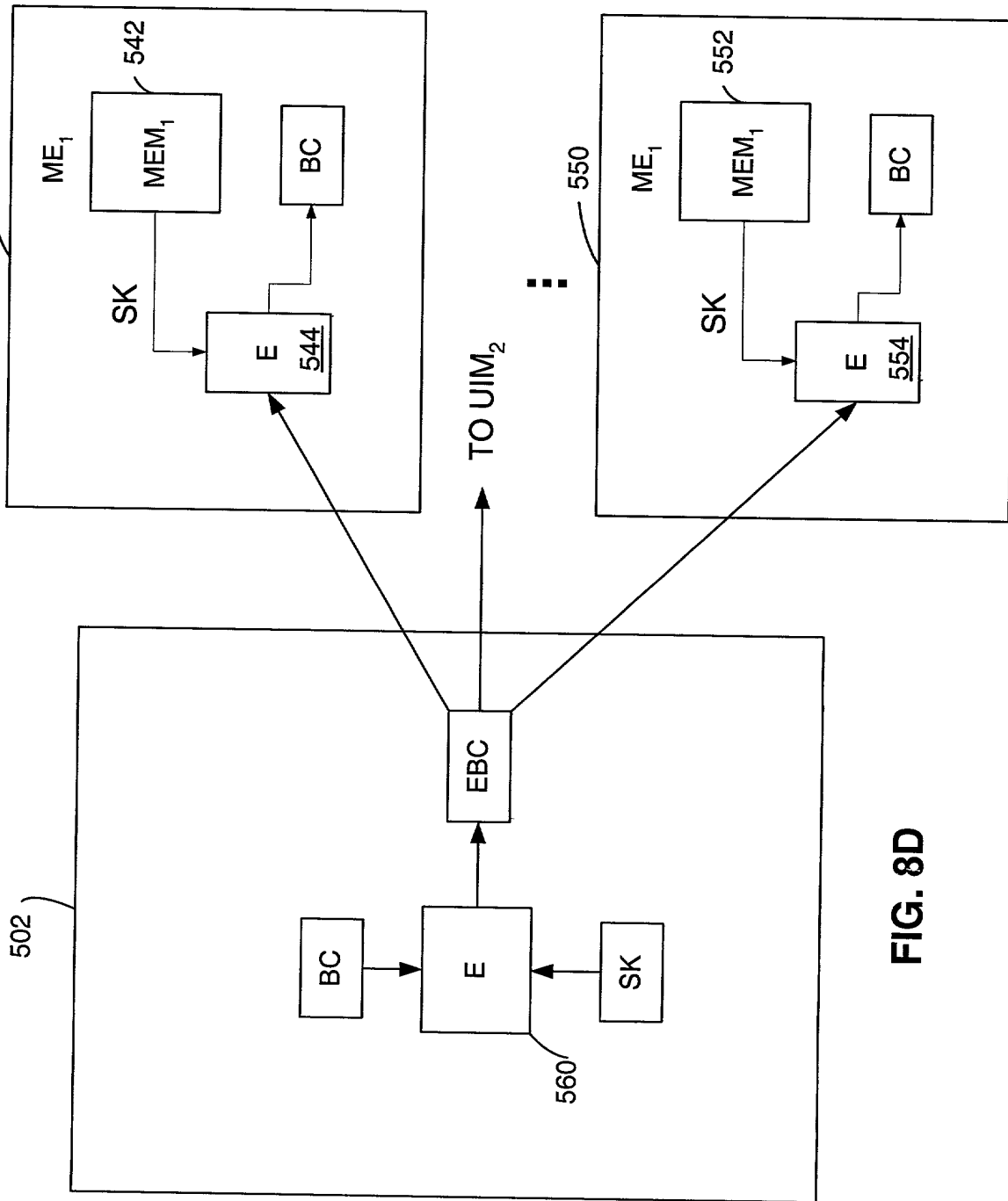


FIG. 8D